Review of the SIA PFAS Consortium Paper on Assembly Test Packaging and Substrates

Lenny Siegel
November 1, 2023

The Semiconductor Industry Association (SIA) PFAS Consortium paper on Assembly Test Packaging and Substrates (ATPS), like its other papers, is designed to show how difficult it would be to eliminate Per- and Polyfluorinated Substances (PFAS) from chip production.

Industry has introduced and embedded a wide variety of PFAS into semiconductor packaging and packages with no consideration of the potential environmental and worker safety risks. In fact, they admit that the absence of regulation is responsible for their lack of knowledge of the use of these chemicals.

The difference for this portion of the production line—as opposed to wafer fabrication—is geography. To my knowledge, there is no assembly, test, and packaging work conducted in the U.S. Most is carried out in East Asia, and much of that is done by assembly subcontractors. This work is relatively labor intensive, compared to wafer fabrication. In general, the dice cut from wafers are attached to packages (substrates) so they can be connected to printed circuit boards and other components,

Given the specialized nature of the chemicals, it is likely that many of the ATPS PFAS are produced in the U.S. and shipped abroad. They are embedded in the final semiconductor products (chips). The paper explains that chipmakers have little idea how much of which PFAS are contained in the final products, but regulating PFAS as a class would force them to begin the lengthy process of identifying and measuring them.

The paper contains mentions of numerous PFAS used in ATPS. There are a lot of them. I found it interesting that PTFE—Teflon—is considered so essential for chip production.

The SIA PFAS Consortium is made up of chipmakers and their suppliers of equipment and materials. To sign up to receive their technical papers, go to
https://www.semiconductors.org/pfas/